What is claimed is:

1. A semiconductor device manufacturing method comprising the steps of:

preparing a wiring substrate including a wiring pattern on a surface;

bonding a connection terminal of an electronic chip, which has a predetermined element and the connection terminal on one surface, to the wiring pattern of the wiring substrate by a flip-chip bonding;

forming a first insulating film on the wiring substrate, the first insulating film having a film thickness that covers the electronic chip, or a film thickness that exposes at least another surface of the electronic chip; and

reducing a thickness of the electronic chip by grinding the first insulating film and another surface of the electronic chip.

2. A semiconductor device manufacturing method according to claim 1, wherein the step of reducing a thickness of the electronic chip is the step of grinding by a grinder, or the step of grinding by the grinder and then polishing by CMP.

3. A semiconductor device manufacturing method according to claim 1, wherein, in the step of reducing a thickness of the electronic chips, a grinding surface of the electronic chip and an upper

surface of the first insulating film are planarized at an almost same height.

4. A semiconductor device manufacturing method according to claim 1, after the step of reducing a thickness of the electronic chip, further comprising the steps of:

forming a via hole having a depth, which reaches the connection terminal on one surface of the electronic chip from a predetermined portion on another surface of the electronic chip, in the electronic chip;

forming a second insulating film on the electronic chip and the first insulating film;

forming a wiring recess, which communicates with the via hole, by etching a predetermined portion of the second insulating film containing a portion that corresponds to the via hole; and

forming a conductive film pattern, which is electrically connected to the connection terminal via the via hole, by filling a conductive film in the via hole and the wiring recess.

5. A semiconductor device manufacturing method according to claim 4, after the step of forming the conductive film pattern, further comprising the step of:

laminating three-dimensionally and packaging a plurality of electronic chips on the wiring

substrate, based on n-times (n is an integer of 1 or more) repetition of a series of steps from the step of bonding the electronic chip by the flip-chip bonding to the step of forming the conductive film pattern connected to the connection terminal via the via hole.

6. A semiconductor device manufacturing method according to claim 4, wherein the wiring substrate has an alignment mark that is formed simultaneously with the conductive film pattern, and

a portion in which the via hole of the electronic chip is formed is identified based on recognition of the alignment mark, in the step of forming the via hole in the electronic chip.

7. A semiconductor device manufacturing method according to claim 4, wherein, in the step of forming the via hole in the electronic chip, a portion in which the via hole of the electronic chip is formed is identified based on recognition of a predetermined pattern on one surface of the electronic chip executed by irradiating X-rays, infrared rays or visible rays from another surface of the electronic chip to transmit therethrough.

8. A semiconductor device manufacturing method according to claim 1, after the step of reducing a thickness of the electronic chip, further comprising the steps of:

forming a via hole having a depth, which reaches the conductive film pattern of the wiring substrate from an upper surface of a predetermined portion of the first insulating film, in the first insulating film;

forming a second insulating film on the electronic chip and the first insulating film;

forming a wiring recess, which communicates with the via hole, by etching a predetermined portion of the second insulating film containing a portion that corresponds to the via hole; and

forming a conductive film pattern, which is connected to the wiring pattern of the wiring substrate via the via hole, by filling a conductive film in the via hole and the wiring recess.

9. A semiconductor device manufacturing method according to claim 8, after the step of forming the conductive film pattern, further comprising the step of:

laminating three-dimensionally and packaging a plurality of electronic chips on the wiring substrate, based on n-times (n is an integer of 1 or more) repetition of a series of steps from the step of bonding the electronic chip by the flip-chip bonding to the step of forming the conductive film pattern connected to the wiring pattern of the wiring substrate via the via hole.

10. A semiconductor device manufacturing method according to claim 5, after the step of laminating three-dimensionally and packaging a plurality of electronic chips on the wiring substrate, further comprising the step of:

forming a passsivation film on or over uppermost electronic chip in the plurality of electronic chips.

11. A semiconductor device manufacturing method according to claim 10, wherein a conductive plug that is connected to the wiring pattern and filled in a through hole which passes through the wiring substrate, is formed in the wiring substrate, and

after the step of laminating three-dimensionally and packaging a plurality of electronic chips on the wiring substrate, further comprising the step of:

forming a bump that is connected to the conductive plug exposed from an opposite surface of the wiring substrate to a surface on which the wiring pattern is formed.

12. A semiconductor device manufacturing method according to claim 10, after the step of forming the passsivation film, further comprising the steps of:

forming a via hole that exposes a part of the wiring pattern, by etching a plurality of interlayer insulating films each consisting of the first

insulating film and the second insulating film, and the passsivation film, on an area which is over the wiring pattern and on the area on which the electronic chip is not mounted;

forming a conductive plug in the via hole; and

forming a bump connected to the conductive plug.

13. A semiconductor device manufacturing method according to claim 10, wherein the wiring substrate is a metal plate including the wiring pattern on a surface, and

after the step of forming the passsivation film, further comprising the steps of:

exposing the wiring pattern by selectively etching the metal plate with respect to the wiring pattern and the first insulating film to remove; and

forming a bump connected to the wiring pattern.

14. A semiconductor device manufacturing method according to claim 10, wherein the wiring substrate is a metal plate including a solder layer filled in concave portions provided to the metal plate, and the wiring pattern formed on the solder layer, and

after the step of forming the passsivation film, further comprising the step of:

forming a bump by selectively etching the metal plate with respect to the solder layer and the first insulating film to remove and to expose the solder layer.

15. A semiconductor device manufacturing method according to claim 11, wherein a structural body in which the electronic chip is laminated and packaged is formed in plural areas of the wiring substrate, and

before or after the step of forming the bump, further comprising the step of:

dividing the wiring substrate such that the structural body in which the electronic chip is laminated and packaged is contained by a predetermined number.

16. A semiconductor device manufacturing method according to claim 1, wherein, in the step of reducing a thickness of the electronic chip, the thickness of the electronic chip is about 150 μm or less.

17. A semiconductor device, in which a plurality of electronic chips which include a predetermined element and a connection terminal, on one surface of the electronic chip, and a conductive film pattern that is connected electrically to the connection terminal via a via hole which passes through the electronic chip, on another surface side of the electronic chip, are laminated and packaged on a wiring substrate including a wiring pattern, in a direction that is perpendicular to a surface direction of the wiring substrate, in a state that

the electronic chips are buried in an interlayer insulating film,

wherein a thickness of the electronic chip is about 150 μm or less, and the connection terminals of the electronic chips are bonded to the wiring pattern of the underlying wiring substrate or the conductive film pattern of the electronic chips by a flip-chip bonding respectively, and the plurality of electronic chips are connected mutually via the via holes in the electronic chips.

18. A semiconductor device according to claim 17, further comprising:

a passivation film formed on or over uppermost electronic chip in the plurality of electronic chips.

19. A semiconductor device according to claim 17, wherein a bump connected to the wiring pattern via a through hole which passes through the wiring substrate, is provided on an opposite surface of the wiring substrate to a surface on which the wiring pattern is formed.

20. A semiconductor device according to claim 18, wherein a bump connected electrically to the wiring pattern of the wiring substrate via a via hole which is formed in the interlayer insulating film and the passivation film on an area which is over the wiring pattern and on the area on which the electronic chip is not mounted, is provided to a

surface of the semiconductor device on which the passivation film is formed.

21. A semiconductor device, in which a plurality of electronic chips which include a predetermined element and a connection terminal, on one surface of the electronic chip, and a conductive film pattern which is connected electrically to the connection terminal via a via hole which passes through the electronic chip, on another surface side of the electronic chip, are laminated three-dimensionally and packaged in a state that the electronic chips are buried in an insulating film,

wherein a thickness of the electronic chip is about 150 μm or less, and the connection terminal of lowermost electronic chip in the plurality of electronic chips is bonded to upper surfaces of a wiring pattern which is buried in an insulating film in a state that lower surface of the wiring pattern is exposed, by a flip-chip bonding, and the connection terminals of other electronic chips in the plurality of electronic chips are bonded to the conductive film pattern of the underlying electronic chip by the flip-chip bonding respectively, whereby the plurality of electronic chips are connected mutually via the via hole in the electronic chips.

22. A semiconductor device according to claim 21, wherein the bump is connected to lower surface

of the wiring pattern to which the connection terminal of the lowermost electronic chip is bonded.

23. A semiconductor device according to claim 17, wherein the conductive film pattern formed on another surface side of the electronic chip is formed to come into contact with another surface of the electronic chip.